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THESIS

PARASITIC FREE
SWITCHED CAPACITOR
COMPOSITE OPERATIONAL AMPLIFIERS

by

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June, 1991

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Parasitic Free
Switched Capacitor
Composite Operational Amplifiers

by

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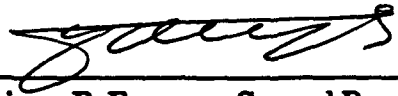
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ABSTRACT

In this research, analog active circuits are analyzed and designed using periodic sampling techniques. Switched capacitor networks are the basis of these techniques. A parasitic free switched capacitor network is combined with composite operational amplifiers to facilitate implementation of low sensitivity, wide bandwidth, analog integrated circuits. The resulting designed network is implemented into a finite gain circuit and into a band pass filter network. The results of these applications are compared with the results obtained from continuous circuits of the same design.

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I. INTRODUCTION

A. OVERVIEW

Operational amplifiers (op amps) are a mainstay of analog and digital circuits. The operational amplifier, however, has limitations that current technology is pressing to improve. Increased bandwidth, reduced passive and active sensitivity, reduced component size, speed and accuracy requirements are at the leading edge of technological requirements. A composite operational amplifier provides a means to improve the bandwidth and the sensitivity of the conventional operational amplifier. Integrated circuits that employ the composite op amp are implemented with continuous resistors. Switched capacitor networks provide the vehicle to replace the continuous resistor in analog and digital circuits and offer significant advantages over continuous resistors.

Switched capacitor networks provide significant improvement in size reduction and accuracy in the manufacture of resistor equivalent circuits. Switched capacitor networks come in many varieties, each offering various strength and weaknesses. Parasitic capacitances have been a serious problem in most switched capacitor networks.

This thesis proposes to combine a parasitic free, switched capacitor network with a composite operational amplifier. The proposed combination will attempt to combine the strengths of wide bandwidth and low passive and active sensitivity of the

composite op amps with the reduced size and high accuracy of the switched capacitor networks. This will provide a practical implementation of an analog integrated c. ..., realizing a parasitic free, switched capacitor composite op amp with superior performance and reduced size compared to most of the existing systems available now.

B. OPERATIONAL AMPLIFIER LIMITATIONS

Single op amps implemented on integrated circuit (IC) chips are widely used in analog and digital circuitry. Technology has increasingly demanded better performance from op amps. Although the op amp provides excellent performance, it has finite limitations in bandwidth performance, sensitivity, speed and accuracy. The gain bandwidth product (GBWP), a product of the finite gain of the amplifier and the 3 dB frequency, is generally considered constant in a single op amp. The sensitivity of the op amp to active components is also well established. Speed, determined by slew rate limits, and accuracy, determined by the input offset voltage, are rarely found in a single op amp.

A new device was developed using a unique combination of op amps to reduce bandwidth limitations, passive and active sensitivity, slew rate and input offset voltage limitations. These devices are called composite operational amplifiers [Ref. 1]. The general design procedure combined N basic op amps (e.g., LM741 or LF 356) into a composite structure . These composite op amps meet or exceed the

existing qualities of the single op amp including stability, sensitivity, Gain Bandwidth Product (GBWP), supply voltage variations and speed.

C. EXISTING PROBLEMS AND SOLUTIONS

The IC implementation of the composite op amp involves resistors which require a significant amount of area on an IC chip. The switched capacitor network provides a means to replace the continuous resistor with a notable savings in area requirements and a significant improvement in manufactured accuracy. The accuracy of the switched capacitor network can be eroded by the inherent and unpredictable error caused by the parasitic capacitances found in the integrated circuit. This is particularly crucial for switched capacitor circuits in that they depend on the relative sizes of their capacitor components to determine the response of the circuit. A parasitic free, switched capacitor network, the modified Open Floating Resistor (OFR), is a network that will eliminate the inherent and unpredictable error present in IC switched capacitor implementations. This modified OFR network, combined with the composite op amp, will provide a circuit that combines high bandwidth, low sensitivity, reduced size and high accuracy into a single network.

D. THESIS ORGANIZATION

The implementation of a parasitic free switched capacitor composite op amp circuit is the goal of this thesis. This thesis will examine the composite op amp in the second chapter. The strengths and weaknesses of the composite op amp will be presented. The third chapter discusses the switched capacitor network. The basis

for switched capacitor network operation will be covered and the problems inherent to a switched capacitor network will be discussed. The fourth chapter will discuss a parasitic free, switched capacitor network that will be utilized in the design of the parasitic free, switched capacitor composite op amp. The fifth chapter combines these components to produce a parasitic free, switched capacitor composite operational amplifier that can be implemented into filter applications. The implemented circuits will be reviewed. The sixth chapter contains the results of the experimental work of this thesis. The seventh chapter draws final conclusions and recommendations for future research.

II. COMPOSITE OPERATIONAL AMPLIFIERS

A. BACKGROUND

Composite amplifiers were developed by S. N. Michael and W. B. Mickhael in 1980. Initial investigations were centered about increasing the GBWP and decreasing the passive and active sensitivity of a single op amp. Active compensation was examined and applied to the design of active filter networks. The resulting composite devices had three external terminals which resembled the input and output terminals of a single op amp.

In the design of two op amp composite amplifiers (C2OA), a nullator-norator pairing [Ref. 1] was used which yielded 136 possible combinations of op amps. Four of the 136 possible combinations yielded acceptable results based on the following criteria:

1. The non-inverting and inverting open loop gains of each of the 136 C2OA's were to have no change in sign in the denominator polynomial coefficients, satisfying the necessary but not sufficient conditions for stability. Also, the need for single op amps with matched GBWP's was to be eliminated resulting in low component sensitivity.

2. The external three terminal performance of the C2OAs were to resemble, as close as possible, the terminal performance of the single op amp.

3. No right half plane zeros due to the single op amp pole were allowed in the closed loop gains of the C2OAs (to minimize the phase shift).

4. The C2OA had to have minimum gain and phase deviation from the ideal transfer function and extended frequency operation to justify the increased number of op amps.

Based on these criteria, the following designs in Figures 2.1 through 2.4 were found to yield the highest response and most accurate results. The open-loop gain input output relationships for these four C2OAs are shown in Table 2.1. The transfer functions, 3 dB frequency equations and the Q equations for the four chosen C2OAs are shown in Table 2.2. [Ref. 2]

Table 2.1 and Table 2.2 provide the mathematical background for the composite op amps used in this research. For this thesis, Q will be chosen to provide a maximally flat gain response. Q and the 3 dB frequency are dependent on the compensation resistor ratio, α and the closed loop gain, K. The necessary and sufficient conditions for stability can be satisfied as shown by the equations in Table 2.3 via the Routh-Hurwitz stability criterion.

B. COMPOSITE OPERATIONAL AMPLIFIER BANDWIDTH IMPROVEMENTS

The bandwidth of the single op amp is finite. The single op amp implemented as a finite gain amplifier has a bandwidth that decreases by a factor inversely proportional to the gain of the circuit. In contrast to the single op amp, the bandwidth of the composite op amps can be made to decrease by a factor inversely proportional to the square root of the gain. This bandwidth improvement is measured for a maximally flat gain response. This maximally flat gain response is achieved when the value of Q is equal 0.707. [Ref. 3] The theoretical frequency response of a negative finite gain composite op amp compared to the frequency response of the single op amp shows an increase in bandwidth of about a decade for high gain applications.

The excellent results and the superior stability properties of the C2OA-1 and the C2OA-2 provide the most attractive configuration for a finite gain implementation from a bandwidth and stability point of view [Ref. 3]. The C2OA-1

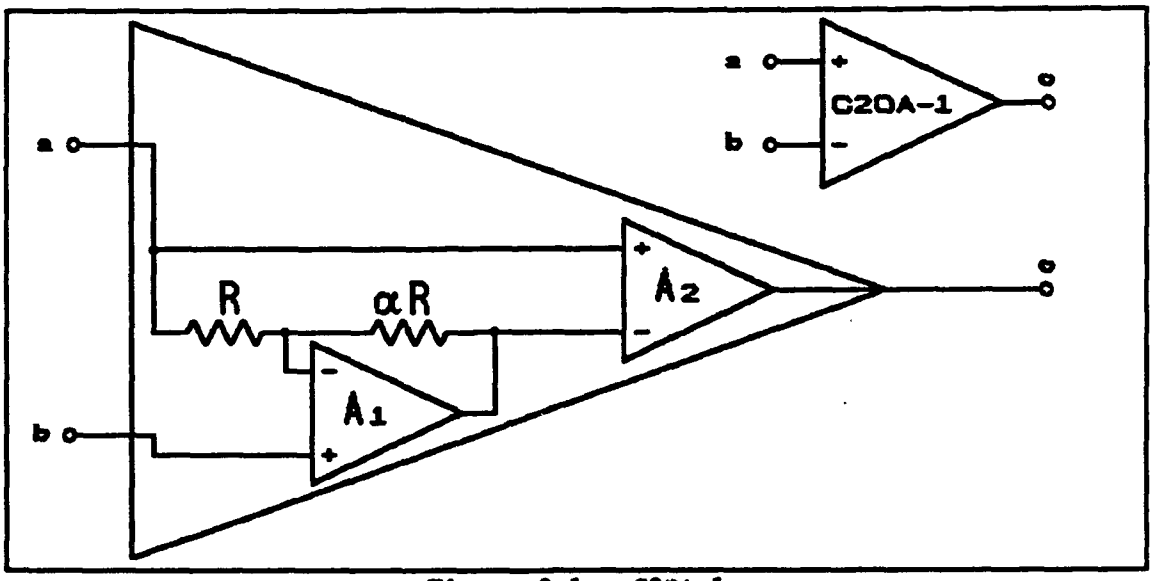

Figure 2.1 C20A-1

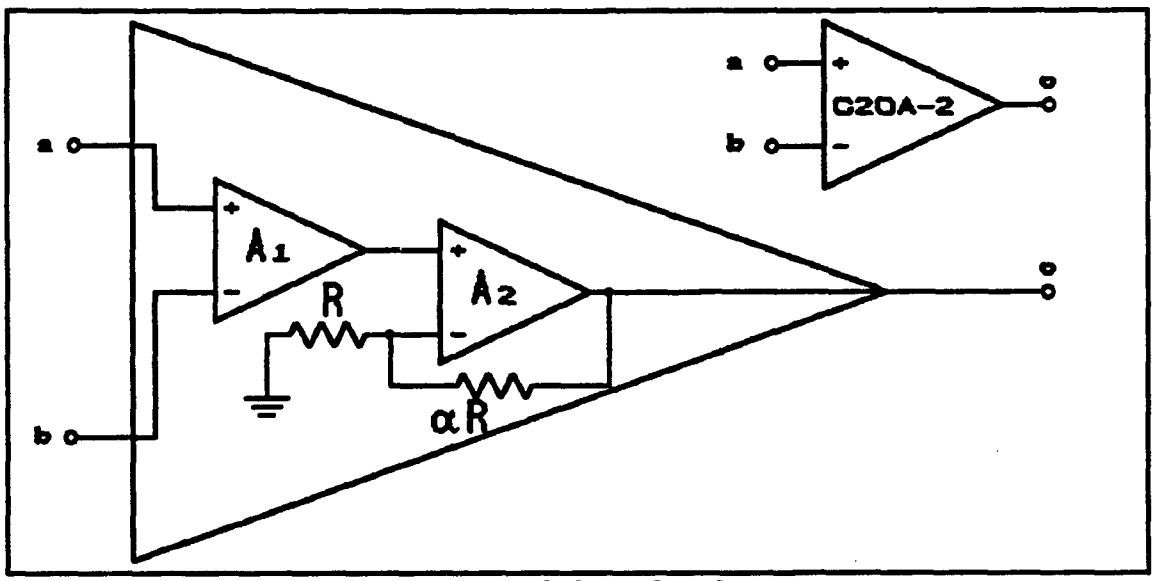

Figure 2.2 C20A-2

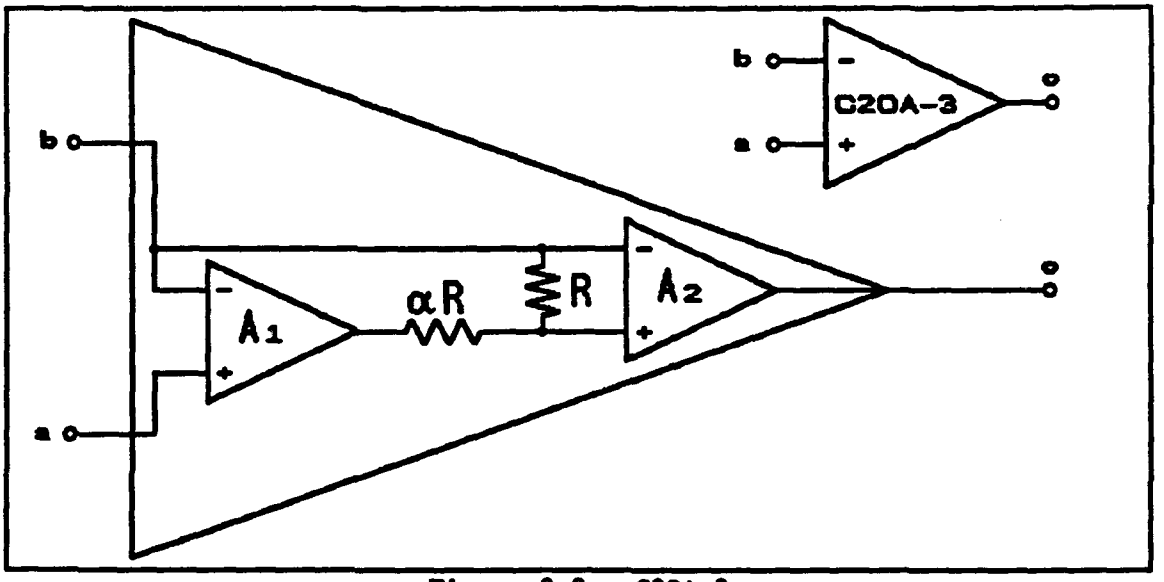

Figure 2.3 C20A-3

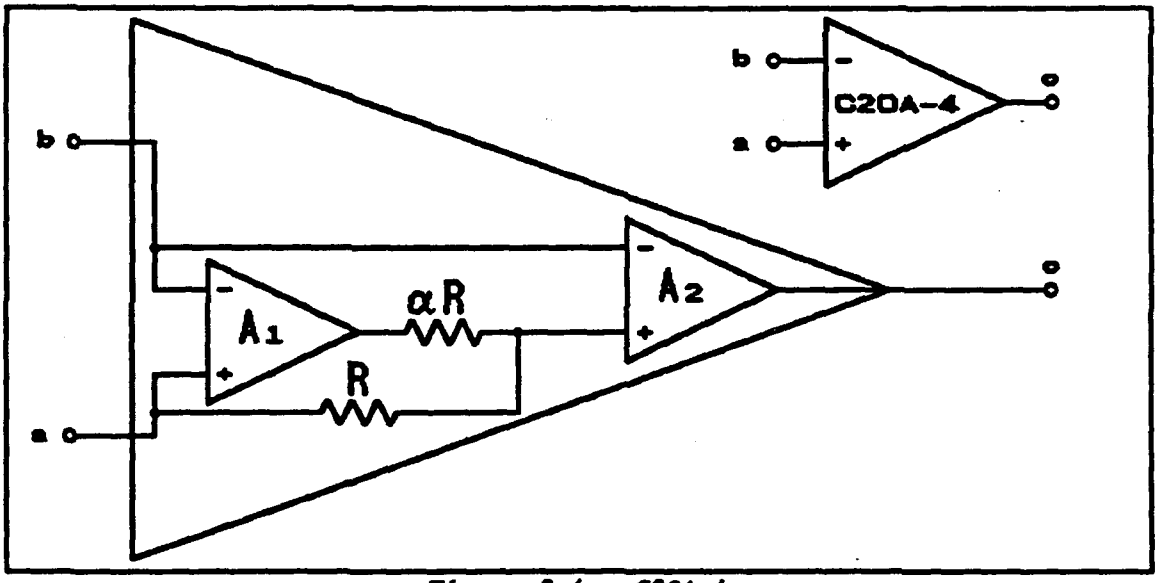

Figure 2.4 C20A-4

TABLE 1 C2OA Open-Loop Gain Input-Output Relationships

$$V_{Oi} = V_a A_{ai}(s) - V_b A_{bi}(s) \qquad (i = 1 \text{ to } 4)$$

forC2OA-1:

$$V_{O1} = V_a \frac{A_2 (1 + A_1) (1 + \alpha)}{A_1 + (1 + \alpha)} - V_b \frac{A_1 A_2 (1 + \alpha)}{A_1 + (1 + \alpha)}$$

forC2OA-2:

$$V_{O2} = V_a \frac{A_1 A_2 (1 + \alpha)}{A_2 + (1 + \alpha)} - V_b \frac{A_1 A_2 (1 + \alpha)}{A_2 + (1 + \alpha)}$$

forC2OA-3:

$$V_{O3} = V_a \frac{A_1 A_2}{A_1 + (1 + \alpha)} - V_b \frac{A_2 (1 + A_1)}{(1 + \alpha)}$$

forC2OA-4:

$$V_{O4} = V_a \frac{A_2 (A_1 + \alpha)}{(1 + \alpha)} - V_b \frac{A_2 A_1 + (1 + \alpha)}{(1 + \alpha)}$$

where α is the internal compensation resistor ratio

TABLE 2 C2OA 3 dB Frequency and Q_p Functions

forC2OA-1:

$$\omega_p = \sqrt{\frac{\omega_1 \omega_2}{1 + K}} \qquad Q_p = \frac{(1 + \alpha)}{\sqrt{1 + k}} \sqrt{\frac{\omega_2}{\omega_1}}$$

forC2OA-2:

$$\omega_p = \sqrt{\frac{\omega_1 \omega_2}{1 + k}} \qquad Q_p = \frac{(1 + \alpha)}{\sqrt{1 + k}} \sqrt{\frac{\omega_1}{\omega_2}}$$

forC2OA-3:

$$\omega_p = \sqrt{\frac{\omega_1 \omega_2}{(1 + k)(1 + \alpha)}} \qquad Q_p = \sqrt{\frac{(1 = k)(1 + \alpha)\omega_1}{\omega_2}}$$

forC2OA-4:

$$\omega_p = \sqrt{\frac{\omega_1 \omega_2}{(1 + k)(1 + \alpha)}} \qquad Q_p = \sqrt{\frac{(1 + k)}{(1 + \alpha)} \frac{\omega_1}{\omega_2}}$$

where α is the internal resistor ratio and ω_p is the three dB point

TABLE 3 Stability Criteria for C2OAs

$1 + \alpha < \frac{1 + K}{2}$	*for C2OA-1/2*
$1 + \alpha < 1 + K$	*for C2OA-3*
$1 + \alpha < 4(1 + K)$	*for C2OA-4*

and the C2OA-2 will be the configurations that will be implemented in the switched capacitor composite op amp circuits of this thesis.

C. COMPOSITE OPERATIONAL AMPLIFIERS SENSITIVITIES

In addition to significant bandwidth improvements, the C2OA configuration also offer a decreased sensitivity to active and passive components. The 3 dB frequency and Q are functions of the GBWPs of the single op amps and α, the value of the ratio between the two resistors in the composite op amp.

The finite gain transfer functions for each of the C2OAs has the general form of

$$\frac{1 + as}{1 + b_1 s + b_2 s^2} \tag{2.1}$$

where

$$b_1 = \frac{s}{\omega_p Q} \tag{2.2}$$

and

$$b_2 = \frac{s^2}{\omega_p^2} \tag{2.3}$$

None of the a or b coefficients are realized through differences which guarantee the low sensitivity of the transfer functions, the 3 dB frequencies and Q to the circuit parameters. The b coefficients are always positive which is a necessary element for the transfer functions stability. Figure 2.6 shows that a mismatch of five percent in the three dB frequencies of the single op amps results in a five percent change in ω_p and a 2.5 percent change in Q.

D. COMPOSITE OPERATIONAL AMPLIFIER OFFSET VOLTAGE AND SLEW RATE

An ideal op amp that has both inputs connected to ground should have an output of zero volts. However, actual op amps exhibit a small DC voltage called the output offset voltage. The voltage required at the inputs of the op amp to force the output to zero is called the offset output voltage. In a typical op amp (e.g., LM741), this input offset voltage is on the order of several millivolts. The output offset voltage is caused by transistor pairs in the input differential stage having different gains and different internal resistances. Every op amp has an offset output voltage.

The offset output voltage of the composite amplifier can be shown to be approximately the offset output voltage of the input op amp, A_1, except in the case of C2OA-1. However, this approximation holds for C2OA-1 also if the value of α is large. The offset output voltages for the four C2OAs are shown in Table 4.

Slew rate defines the rate of change in the output voltage due to an instantaneous input voltage change in an op amp. The slew rate is dependent on the bias current and the compensation capacitor value. Increasing the slew rate of a single op amps results in the increase of the offset voltage. A single, fast, accurate op amp is impossible to obtain because of slew rate and output offset voltage limitations. A high slew rate, fast settling, wide bandwidth op amp in the A_2, output, position will provide a fast output stage and hence a fast composite op amp.

TABLE 4 C2OA Input Offset Voltages

C2OA-1	$V_{off} = V_{off1} + (V_{off2} / \alpha)$
C2OA-2	$V_{off} = V_{off1} + (V_{off2} / A_1)$
C2OA-3	$V_{off} = V_{off1} + (V_{off2} (1 + \alpha) / \alpha)$
C2OA-4	$V_{off} = V_{off1} + (V_{off2} (1 + \alpha) / \alpha)$

The slew rate and bandwidth of the A_1 op amp have little effect on the output of the composite amplifier. Therefore no distortion or dynamic range limitations due to the limited performance of the input op amp is seen on the composite amplifiers output. The composite op amp shows all the output performance characteristics of the A_2 op amp.

Thus a high-speed, high accuracy, composite amplifier can be constructed using a low input offset voltage op amp as the input stage and a high slew rate amplifier as the output stage. This combination can be realized, only due to the fact that the GBWP mismatch of the op amps utilized in the C2OA is tolerated.

Such a high-speed, high-accuracy composite amplifier could prove to be very useful in A/D and D/A converters, switched capacitor networks, as well as many other applications.

E. CONCLUSIONS

This chapter contrasted the composite op amp with the single op amp. Superior performance in the areas of GBWP and sensitivity are the primary motivations for the implementation of this system in the switched capacitor network. The improved offset voltage and slew rate performance provides additional flexibility

in the utilization of the composite op amp in switched capacitor applications. A brief orientation to switched capacitor networks will be presented in the next chapter.

III. SWITCHED CAPACITOR NETWORKS

A. GENERAL

Modern active filter design has been based mainly on RC filters. Practical RC filter design generally includes large value capacitors and high precision resistors to achieve accurate time constants. Large value capacitors and high precision resistors have been a major obstacle in integrated circuit (IC) implementation of active filters.

Switched capacitor networks provide several advantages in IC manufacturing. A primary advantage is that the switched capacitor equivalent resistor typically requires only a fortieth of the area needed for a continuous resistor [Ref. 4]. A second primary advantage is gained in the accurate prediction of manufactured component values. Precise values of C and R are required for the accurate prediction of Q and to obtain accurate realization of the RC time constant. In addition to being area expensive, integrated resistor inaccuracies are about 25% and often require expensive laser trimming. IC implementation of a switched capacitor network can produce an equivalent resistor with a comparative capacitor accuracy of .1%.

MOS integrated circuit technology has found wide application in industry because of its superior logic density compared to that achievable with bipolar technologies. A unique property of MOS integrated circuits is the capability to store

charge on a node for a few milliseconds and to sense this charge continuously and nondestructively [Ref. 5].

The realization of the RC time constant can be controlled in MOS SC technology by determining the clock period and the capacitor ratios. This idea made feasible the implementation of accurate active filters in IC form. In addition, MOS components are nearly ideal with very low power dissipation and good temperature stability. Sampled data filters can be fabricated by using NMOS and CMOS processing [Ref. 4]. Digital and analog circuitry can be placed on the same chip. These factors make the successful IC implementation of switched capacitor filters very attractive.

B. SWITCHED CAPACITOR IMPLEMENTATION

A switched capacitor circuit is composed of switches, capacitors and a clock. The symbolic notation for this thesis is now identified. The switch symbols will always be shown in the open position. The system has an n-phase clock, where there are n segments in the clock period T. For this thesis a two phase clock will be used. Each switch of the circuit is associated with a clock phase designated by ϕ_k where k is an integer representing the number of phases of the clock ranging from 1 to n. Typically a switch closes only once per clock cycle. It is imperative in switched capacitor networks that no two switches driven by different phases of the clock be closed simultaneously, resulting in a short circuit. Therefore it is necessary that each phase of the clock has less than a 50% duty cycle. This results in a clock with

nonoverlapping phases. A bipolar two phase nonoverlapping clock is shown in Figure 3.1. A convenient phase notation is denoted by defining odd as Φ_1 and defining even as Φ_2. Thus the sampled data wave forms can be stated as the sum of their even (e) and odd (o) components.

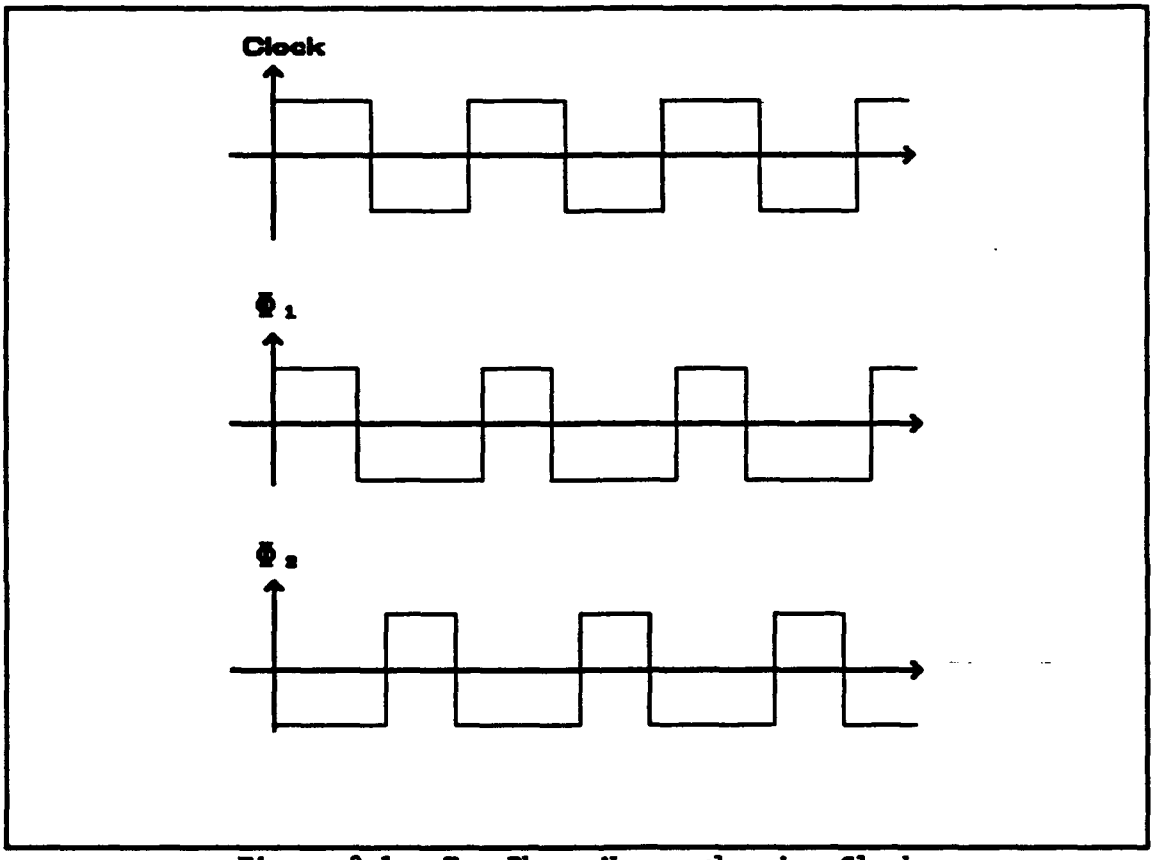

Figure 3.1 Two Phase Nonoverlapping Clock

The transfer function of a switched capacitor network can be represented by four different transfer functions which correspond to the even and odd phases for both input and output. A useful notation for the transfer function is shown in Equation 3.1, where i and j can either be e or o.

$$H^{ij}(z) = \frac{V^j_{out}(z)}{V^i_{in}(z)} \qquad (3.1)$$

Switched capacitor networks have sampled data characteristics and can be treated similar to digital filters and analyzed in the z-domain. However, switched capacitor networks are analog, thus the concepts of impedance and load which are absent in the digital filters are retained. To resolve this problem and to be able to apply network theory, z-domain equivalent circuits, known as building blocks, are used. Each switched capacitor unit has a corresponding z domain equivalent circuit or building block. These building blocks can then be joined together to form an overall z domain equivalent circuit

C. SWITCHED CAPACITOR EQUIVALENT RESISTORS

Switched capacitor equivalents of a continuous resistor can be obtained by several methods. The goal is to replace the resistor with a switched capacitor equivalent that exhibits the same performance characteristics as the continuous resistor. Several methods have been developed for continuous resistor realization. One of these methods, the parallel switched capacitor realization of a resistor is shown in Figure 3.2. Initially both switches are open and the capacitor is without charge. During the odd phase, the switch at Φ_1 is closed and the capacitor charges to V_1 as shown by

$$Q\,(t_0 + T/2) = C\,V_1 \qquad (3.2)$$

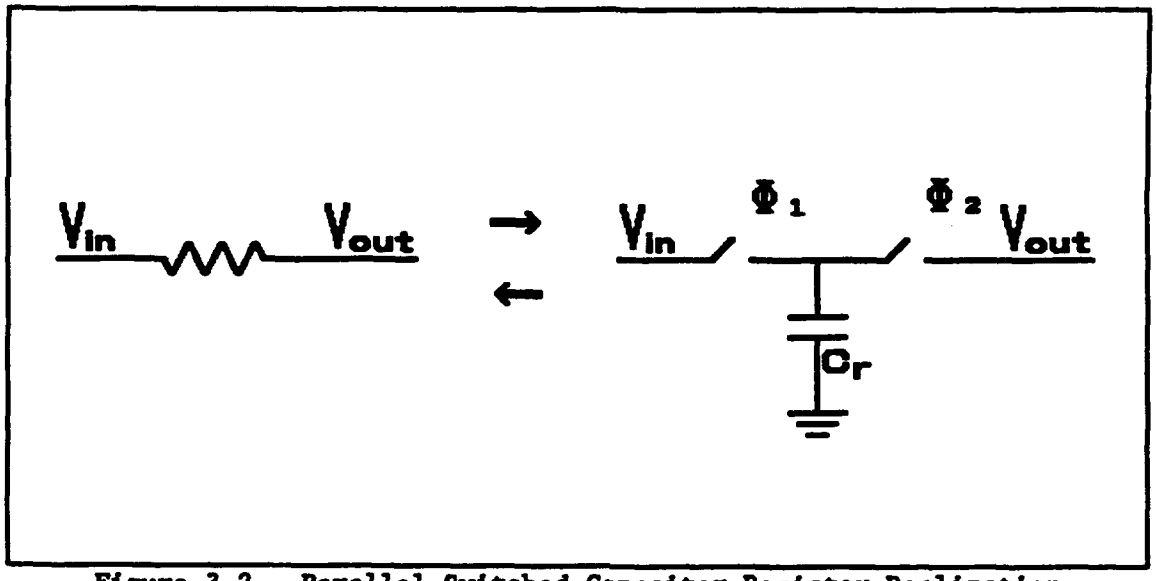

Figure 3.2 Parallel Switched Capacitor Resistor Realization

The nonoverlapping clock then opens the Φ_1 switch before it closes the Φ_2 switch. When Φ_2 is closed, C is charged to V_2. During this phase the charge is

$$Q\,(t_0 + T) = C\,V_2 - C\,V_1 \qquad (3.3)$$

The final charge on the capacitor during a phase is not necessarily equal to the charge flowing past the voltage sources during that period. The current can be expressed as

$$i = dq / dt \tag{3.4}$$

where

$$dq = C\, dV \tag{3.5}$$

For $dV = V_2 - V_1$, (3.5) becomes:

$$dq = C(V_2 - V_1) \tag{3.6}$$

which when averaged yields

$$I = \frac{C(V_2 - V_1)}{T} \tag{3.7}$$

or

$$\frac{(V_2 - V_1)}{I} = \frac{T}{C} \tag{3.8}$$

which yields the following relationship for parallel realization:

$$R = \frac{T}{C} \tag{3.9}$$

where T is the clock period.

The relationship of the clock frequency to the signal frequency is a critical element in the switched capacitor network. The clock frequency is related to the switched capacitor frequency by modifying Equation 3.9 to become

$$R = \frac{1}{f_c C} \tag{3.10}$$

where

$$f_c = \frac{1}{T} \tag{3.11}$$

This equation holds as long as the clock frequency is much larger than the signal frequency or

$$f_c >> 2 \pi f \tag{3.12}$$

so that the signals at the voltage sources, V_1 and V_2, can be assumed to be constant over the clock period, T. Also, if the switched frequency is much higher than the signal frequency, the time sampling which occurs in the circuit can be ignored [Ref. 6]. In this case the switched capacitor equivalent resistor can generally be considered as a direct replacement for the continuous resistor. When the switch frequency is much larger than the signal frequency the signal is approximately

constant and the current for the circuit can be expressed as in Equation 3.7. RC time constants are directly affected by the clock frequency according to

$$\tau = R\,C = \frac{C}{f_c\,C_R} \qquad (3.13)$$

where C_R is the switched capacitor value. This gives great potential for programming a switched capacitor output according to the input clock frequency. The clock frequency in this research was chosen to be an order of magnitude greater than the signal frequency, which is based upon a maximum signal frequency of 100 KHz.

D. CHARGE CONSERVATION ANALYSIS

This method of switched capacitor analysis is slightly different than Kirchoff's current law. In this method, the charge q is used instead of the current i. Because of the two phase nonoverlapping clock operation, a pair of charge conservations are realized which characterize the charge condition of each node for each sample instant. A pair of equations consists of both the equation for the even sampling times and the odd sampling times. The pair of equations for a two phase clock are

$$q_1^e(t') = q_2^e(t) + q_C^{e,o}(t) \qquad t' > t \qquad (3.14)$$

for an even clock phase, ϕ_2 and

$$q_1^o(t') = q_2^o(t) + q_C^{o,e}(t) \qquad t' > t \qquad (3.15)$$

for an odd clock phase, Φ_1, where $q_1(t')$ is the charge on the node at the reference time, $q_m(t)$ is the charge on the node remaining from the previous phase, and $q_c(t)$ is the new charge added to the particular node.

Switched capacitor networks are mainly characterized by their transfer functions which have the discrete time voltage v(kT), and discrete time charge differentiation $\Delta q(kT)$ as variables. Assuming a switched capacitor network with i capacitors, where the total number of capacitors is N, connected to a node P during even and odd clock phases, the charge at the node can be expressed as

$$\Delta q_p^e(nT) = \sum_i q_{pi}^e(nT) - \sum_i q_{pi}^e[(n-1)T] \qquad (3.16)$$

for even n, and $i = 1,2,...N_{ep}$.

$$\Delta q_p^o(nT) = \sum_i q_{pi}^o(nT) - \sum_i q_{pi}^o[(n-1)T] \qquad (3.17)$$

for odd n, and $i = 1,2,...N_{op}$.

In the z-domain the above charge equations can be written as

$$\Delta Q_p^e(z) = \sum_i Q_{pi}^e(z) - z^{-1/2} \sum_i Q_{pi}^o(z) \qquad (3.18)$$

where $i = 1,2,...,N_{ep}$ and

$$\Delta Q_p^o(z) = \sum_i Q_{pi}^o(z) - z^{-1/2} \sum_i Q_{pi}^e(z) \qquad (3.19)$$

where $i = 1,2,...,N_{op}$.

E. EXPERIMENTAL DEMONSTRATION OF SWITCHED CAPACITORS AS EQUIVALENT RESISTORS

Experimental verification of the theoretical and mathematical equivalent resistance relationship between switched capacitor networks for which the output signal was a sampled analog signal was done previously [Ref. 5]. The two phased clock required for the switched capacitor network realizations is generated from a single clock in a circuit shown in Figure 3.3. This circuit produces the two phase nonoverlapping clock required by the switched capacitor networks and is used throughout this thesis. The NOR gate output is high only when both inputs are low, which ensures that when one phase is high that the other phase will be low. The circuit elements used in the lab are composed of a Hewlett Packard 3312A Function Generator which generates a bipolar square wave input clock signal, CD4049CN CMOS bipolar gates for the inverters, and the CD4001BEX CMOS bipolar gate which provides the NOR gate. The inverters have a switching delay of approximately 20 ns and the NOR gate has a switching delay of approximately 20 ns.

The actual delay in the assembled circuit was found to be 60 ns as predicted. Although the CMOS switches have a maximum switch rate of approximately 5 MHz; the clock switching delay combined with the 65 dB gain limits of the amplifier, and a anticipated maximum signal frequency less than 100 KHz, prompted the use of a 1 MHz clock to drive the switched capacitor circuits in this research. In previous

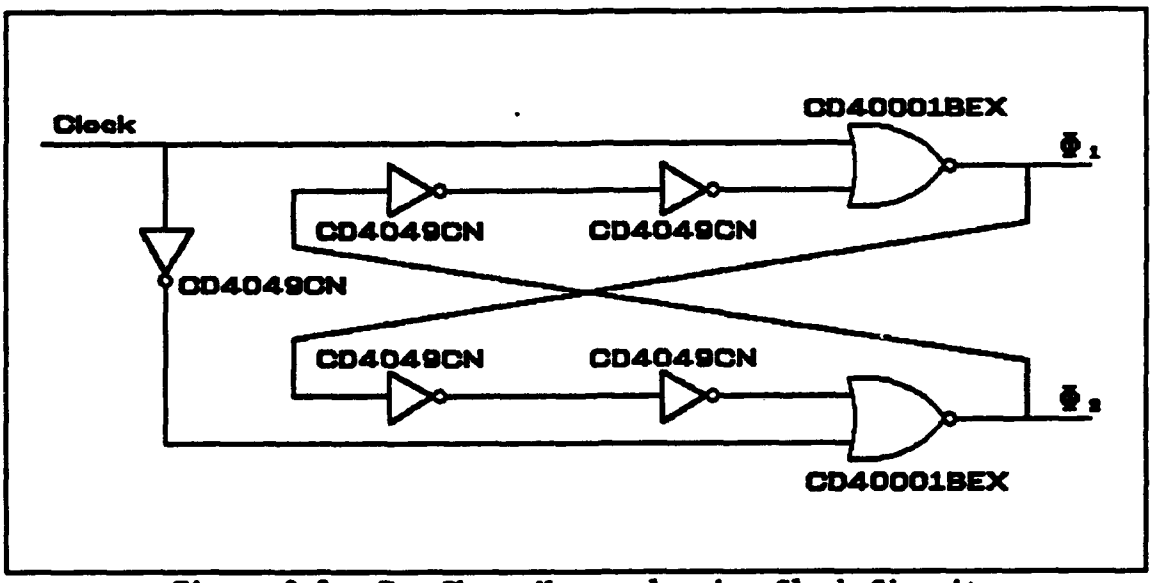

Figure 3.3 Two Phase Nonoverlapping Clock Circuit

work a simple voltage divider was constructed to demonstrate how closely the experimental results matched the computed values [Ref. 5]. The switches used in the switched capacitor networks were MC4066B CMOS bilateral switches. These switches are used throughout this research. The lower channel resistance (80 ohms maximum) makes these devices suitable for switched capacitor networks and are used in all stages of this research. The experimental results showed some deviation between the switched capacitor networks and the computed values. These deviations are caused by nonideal properties of the switched capacitors.

It was shown experimentally in [Ref. 5] that only a particular range of ratios of capacitors and clock frequencies provided accurate results for the switched capacitor realizations. The variations were due to parasitic capacitances inherently present in the components. Methods for dealing with parasitic capacitances will be discussed in the next chapter.

The bilinear realization from [Ref. 5] yielded the best results from among the realizations tried, but were still hampered by the parasitic capacitances inherent in the design. Because of the parasitic capacitances, the final equivalent resistor values were found to be lower than predicted. Under proper conditions, however, the parasitic capacitances of a switched capacitor network can be nullified which will bring the equivalent resistances back to the expected values.

F. NONIDEAL PROPERTIES OF SWITCHED CAPACITORS

The use of CMOS FET as switches introduces some secondary effects to the switched capacitor networks. These effects may be classified as follows:

1. clock feed through
2. offset error and noise
3. nonlinear P-N junction capacitance
4. Incomplete transfer of charge

The clock feed through will be discussed in the following chapter. Offset error and noise are not addressed in this thesis. The nonlinear P-N junction capacitance and the incomplete transfer of charge are forms of parasitic capacitances and will be discussed in the next chapter.

IV. PARASITIC FREE SWITCHED CAPACITOR NETWORKS

A. GENERAL

Switched capacitor networks provide several advantages in IC manufacturing. A primary advantage is gained in the accurate prediction of manufactured component values. Precise absolute values of C and R are required for the accurate implementation of Q and the realization of precise corner frequencies. In addition to being area expensive, resistors are accurate to only about 25% and may require expensive laser trimming. IC implementation of a switched capacitor network can produce an equivalent RC product with a comparative accuracy of .1%. This is due to the fact that this quantity is determined by capacitor ratios in switched capacitor realizations, as explained in the previous chapter. The resistor values in a switched capacitor composite op amp vary by a factor of α, so the switched capacitor composite op amp can be manufactured with this same comparative accuracy. This accuracy, however, is achieved only if the parasitic capacitances can be nullified or removed. Parasitic capacitances are unpredictable and can significantly affect the performance of a switched capacitor network. Switched capacitor parasitic capacitances cannot be removed with present technology; however, they can be nullified with a modified circuit topology. The goal of this chapter is to show a parasitic free switched capacitor topology and demonstrate its properties.

B. PARASITIC CAPACITANCES

In integrated circuits, charge differences exist between the silicon layers comprising the substrate and the plates of the capacitor. These charge differences are inherent to the construction of the components which causes unpredictable error to be introduced into the designed component. These charges are manifested as parasitic capacitances that are present in the integrated circuit. Figure 4.1 from [Ref. 7] shows the parasitic capacitances associated with an integrated circuit capacitor. Parasitic capacitances exist between the bottom plate of the capacitor and the substrate, C_b, and between the top plate of the capacitor and the substrate, C_t. The top plate parasitic capacitance includes the metal connections from the top plate to other components and the nonlinear capacitance of the source-drain diffusions of the switches. The value for the parasitic capacitances between the top plate and the substrate is typically between 10 and 20 percent of the design value of the capacitor. The parasitic capacitance associated with the top plate of the capacitor is between one and five percent of the design capacitor value. A typical method of nullifying the effects of the bottom plate capacitance is to connect the bottom plate to ground, an independent voltage source or an op amp output.

Additional parasitic capacitances are introduced by the gates that perform all the switching in the network. These parasitic capacitances are manifested through the gate-source capacitance and the gate-drain capacitance. In addition to adding parasitic capacitances, the CMOS switches although not a part of the signal transmission, allow the coupling of switching noise of the clock phases ϕ_1 and ϕ_2 to

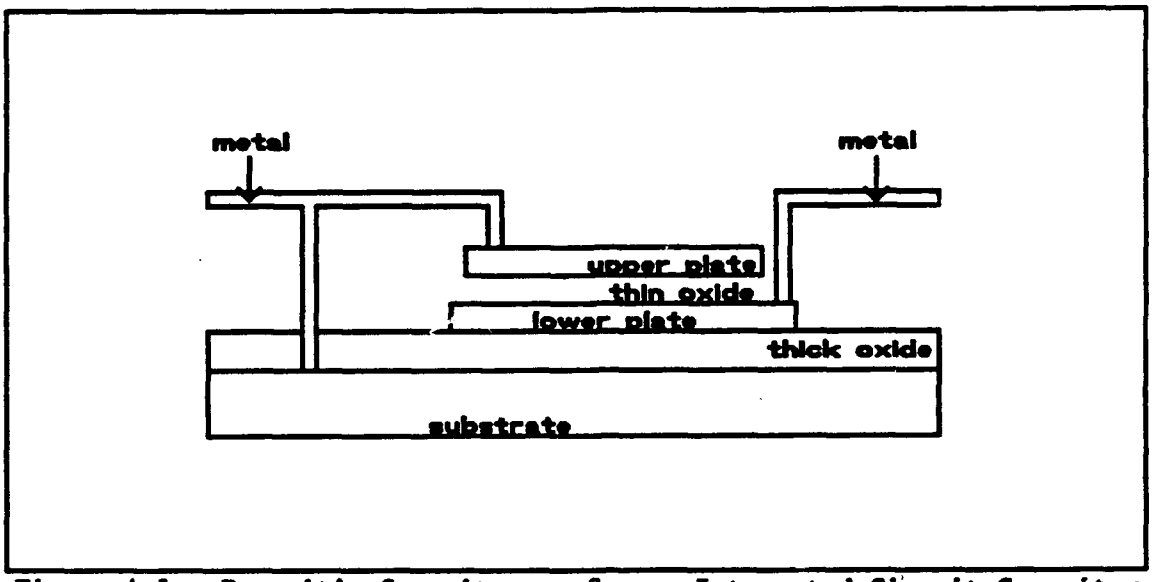

Figure 4.1 Parasitic Capacitances for an Integrated Circuit Capacitor

the signal resulting in clock feedthrough. Figure 4.2 shows a switched capacitor integrator circuit implemented with CMOS switches. Figure 4.3 shows this circuit with the associated parasitic capacitances. The parasitic capacitances of this circuit are reduced to the effective parasitic capacitances of Figure 4.4 by the following arguments.

The capacitors between the inverting input of the op amp and the switch are at virtual ground and thus always shorted. The parasitic capacitances between the output of the op amp and ground as well as the parasitic capacitances that are driven by the voltage source are inconsequential. The effective parasitic capacitances that actually contribute to the circuits parasitic inaccuracies are shown in Figure 4.4. The error that is introduced by the parasitic capacitances of Figure 4.4 is given by

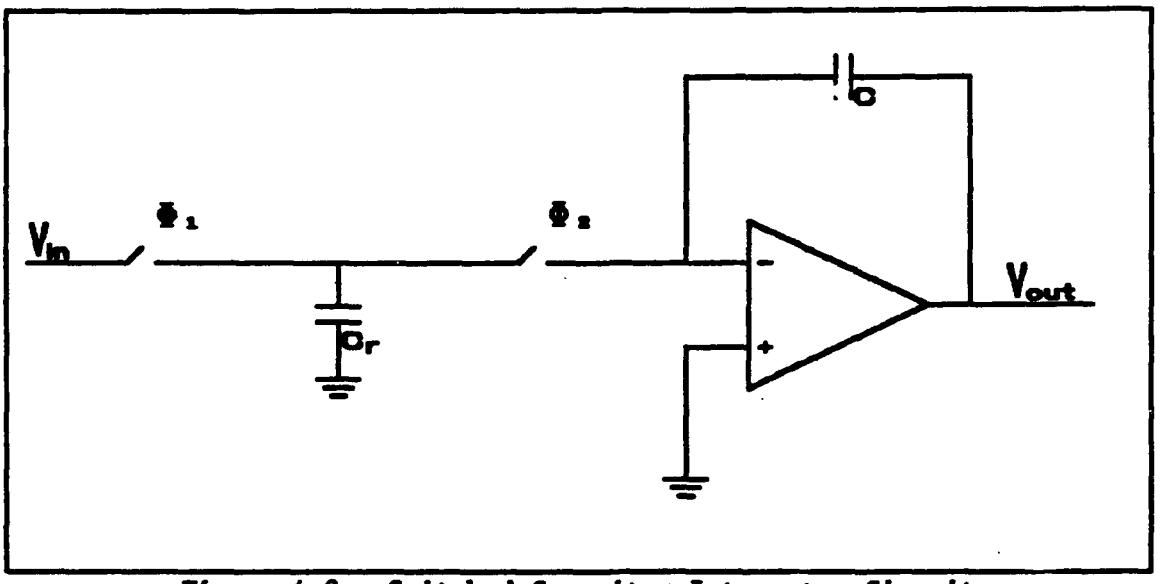

Figure 4.2 Switched Capacitor Integrator Circuit

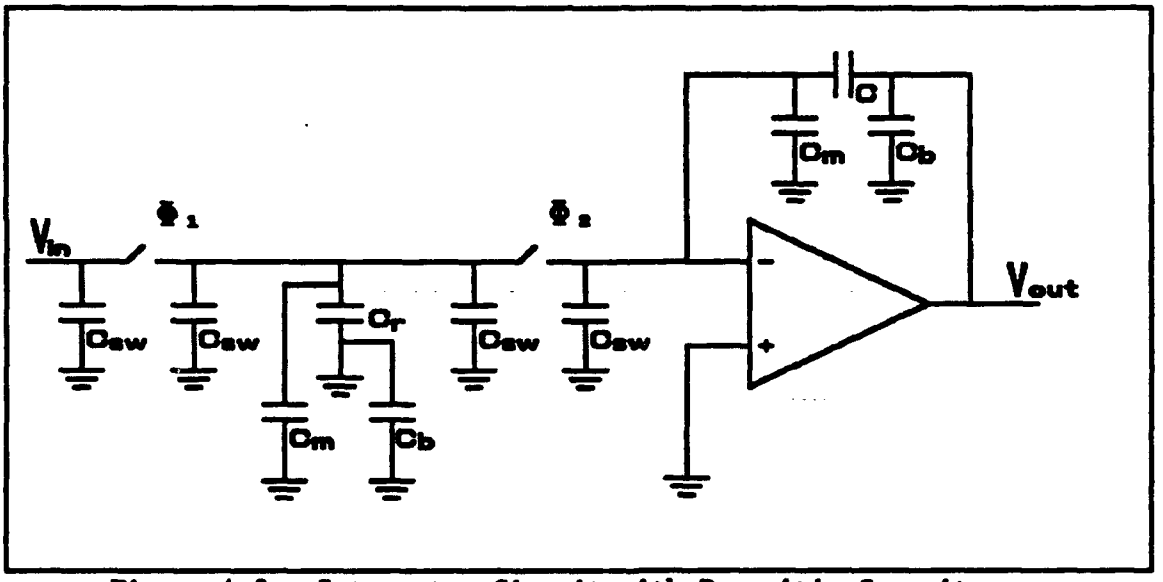

Figure 4.3 Integrator Circuit with Parasitic Capacitances

$$\frac{V_{out}^{e}}{V_{in}^{e}} = \frac{\frac{C_1}{C_2}\left(1 + \frac{C_2}{C_1}\right) z^{-1/2}}{1 - z^{-1}} \qquad (4.1)$$

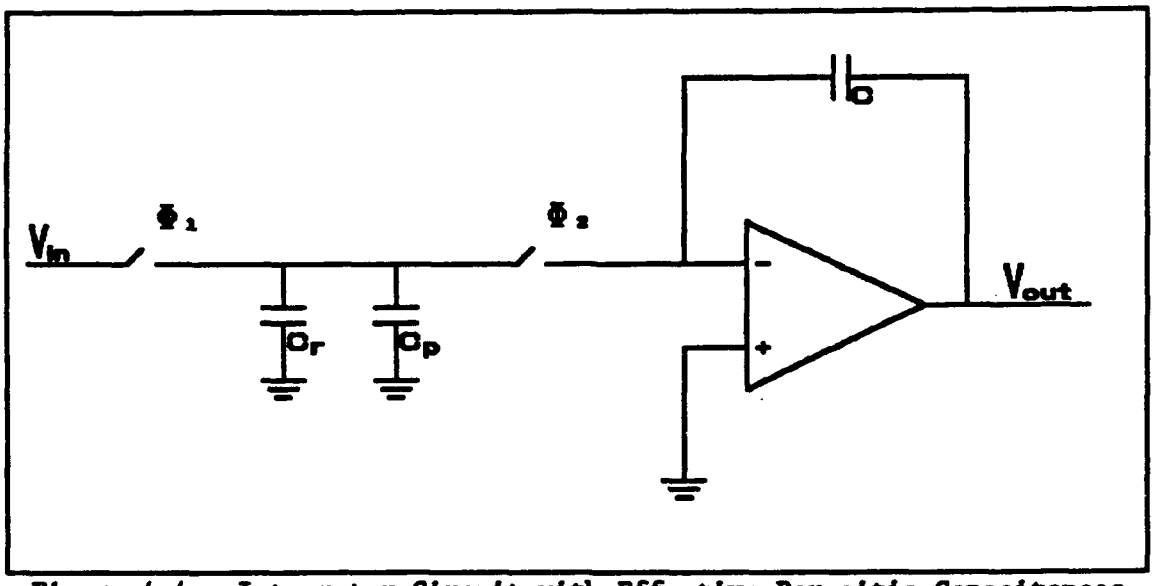

Figure 4.4 Integrator Circuit with Effective Parasitic Capacitances

where the gain error is

$$1 + \frac{C_p}{C_1} \qquad (4.2)$$

which can be significant. By modifying the circuit topology, the effects of the remaining parasitic capacitances in the circuit can be nullified. The succeeding section will show the component placement for the modified circuit topology and demonstrate the parasitic free switched capacitor network.

C. A PARASITIC FREE SWITCHED CAPACITOR NETWORK

Several practical considerations must be taken into account when designing any MOS switched capacitor network. When implementing a switched capacitor realization of a resistor in the feedback loop of an op amp, an open loop situation

can occur because the two phase nonoverlapping clock ensures the switch closings for each phase do not overlap, which causes stability problems. This stability problem can be overcome with the addition of an unswitched capacitor in parallel with the switched capacitor equivalent resistor. In addition, no op amp input node can have only capacitors attached, but a DC path to ground or a voltage source must be provided for op amp biasing purposes. To facilitate the reduction of parasitic capacitances, the bottom plate of the capacitors should be grounded or connected to a voltage source via a switch. This will eliminate the 10 to 20 percent parasitic capacitance induced between the bottom plate and the substrate. Also the noninverting terminal of the op amp should be connected to a constant voltage source to avoid common node rejection problems that introduced by the coupling between the two input terminals.

A modified circuit topology of the integrator circuit of Figure 4.5 eliminates the effects of parasitic capacitances found in the switched capacitor equivalent resistor. Placing two addition switches for each switched capacitor equivalent resistor, as shown in Figure 4.5, will nullify the effects of the parasitic capacitances in this circuit. This switched capacitor equivalent resistor configuration is called the modified Open Floating Resistor (OFR) configuration. This configuration can be demonstrated to parasitic free.

The parasitic capacitances associated with Figure 4.5 are shown in Figure 4.6. The effective parasitic capacitances of the integrator circuit in Figure 4.6 can be found by removing those parasitic capacitances connected between ground and

ground, as well as those connected between ground and a voltage source as done for the integrator circuit of Figure 4.3. The remaining parasitic capacitances of the integrator circuit are shown in Figure 4.7. The remaining parasitic capacitances are rendered inconsequential by the two additional switches which are controlled by the nonoverlapping two phase clock.

Figure 4.8 shows the positions of the gates at ϕ_2. During the switch closure at ϕ_2 the capacitor is completely discharged to ground removing any untransferred charge remaining on the node. During clock phase ϕ_1 the capacitor is charged to the applied voltage difference, as shown in Figure 4.9, allowing the transfer of charge through the node. During ϕ_2, C_r is charged to

$$q = (V_{in} - V_{out}) \tag{4.3}$$

This cycle is then repeated. For a switching rate of T, the average current through the branch is

$$i = \frac{C}{T} (V_{in} - V_{out}) \tag{4.4}$$

Similarly a non-inverting parasitic free switched capacitor integrator can also be realized as shown in Figure 4.10 using an OFR switching arrangement.

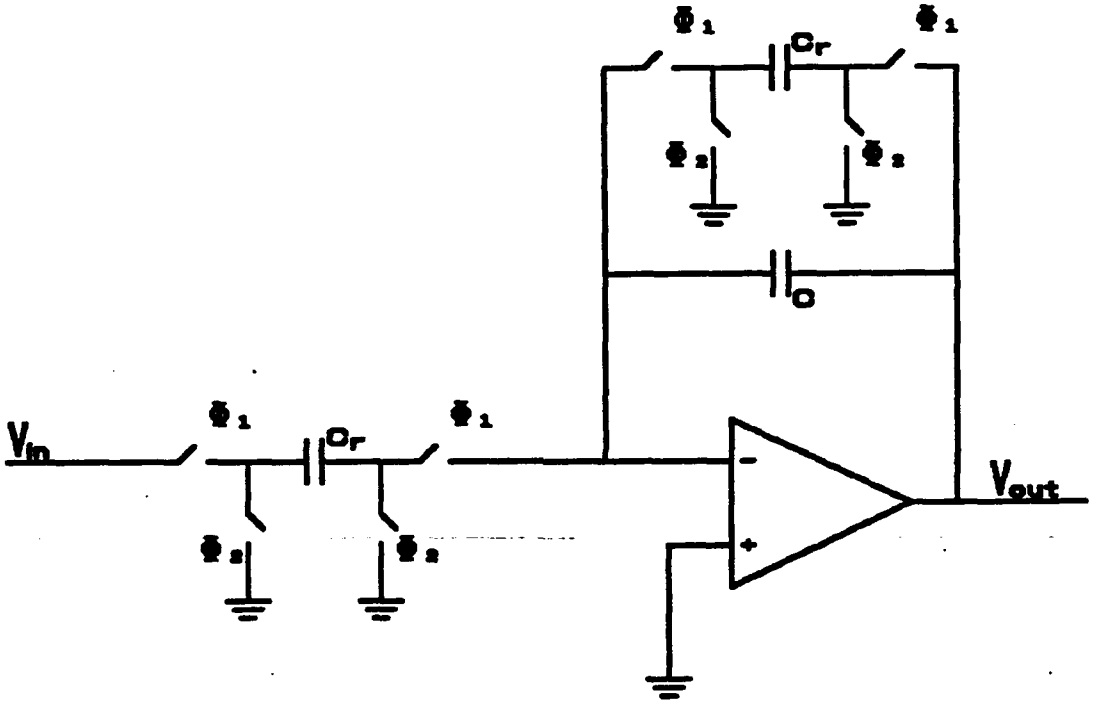

Figure 4.5 Modified OFR Switched Capacitor designed Integrator Circuit

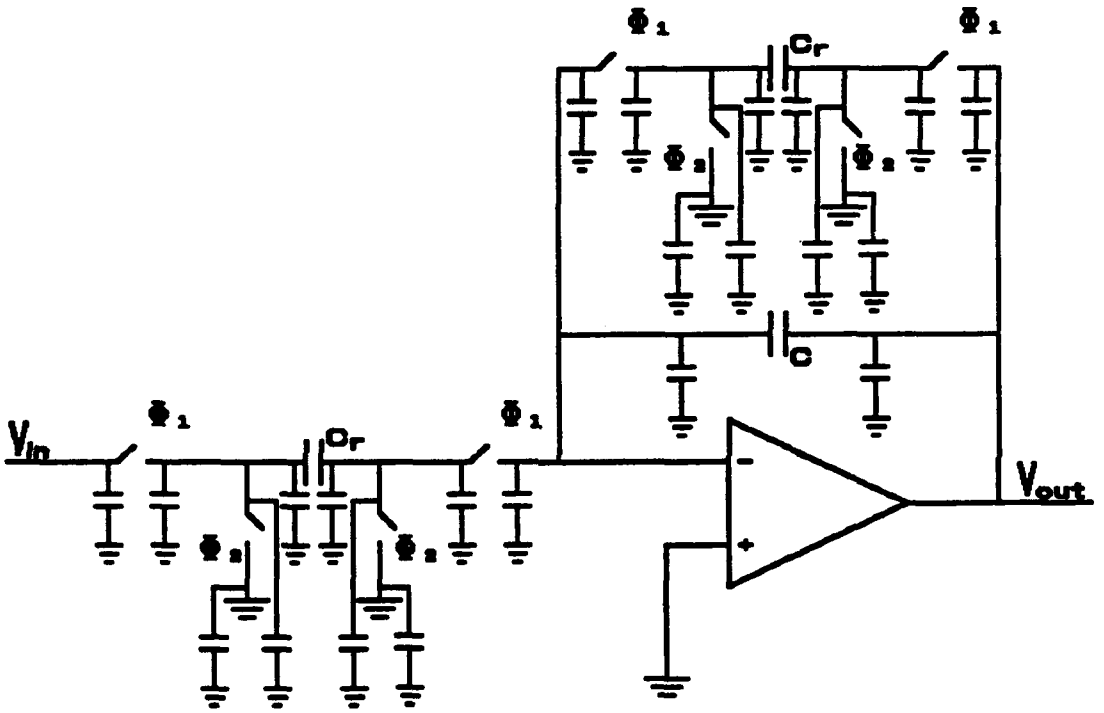

Figure 4.6 Parasitic Capacitances in OFR Switched Capacitor Integrator Circuit

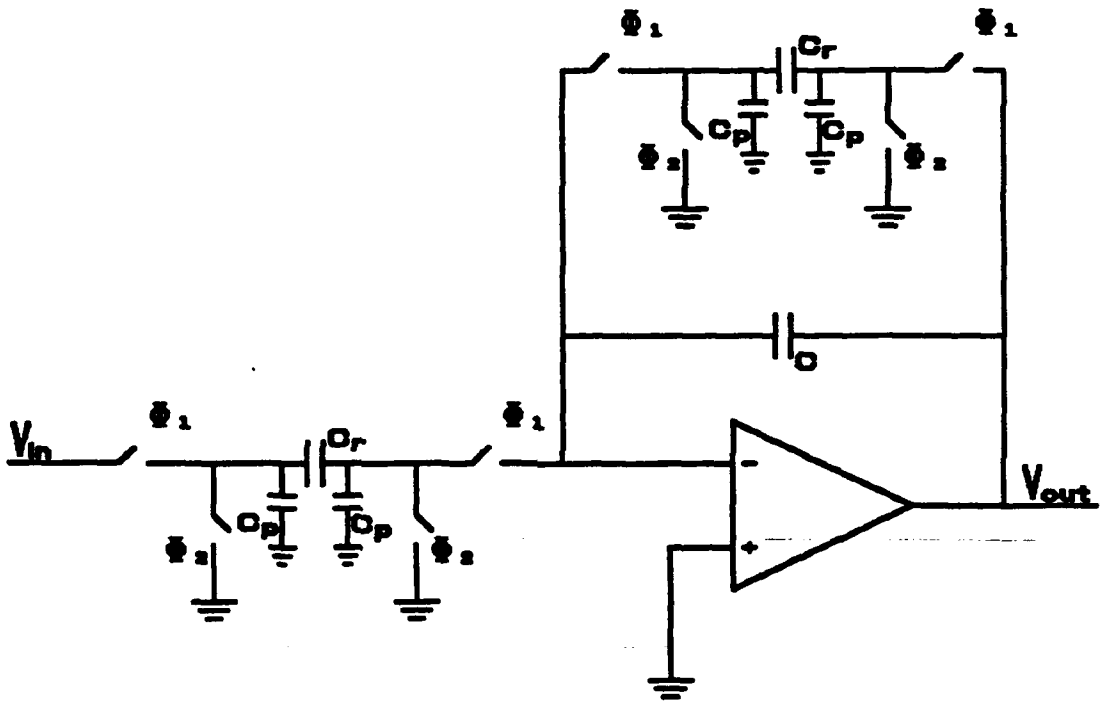

Figure 4.7 Effective Parasitic Capacitances of OFR Switched Capacitor Integrator Circuit

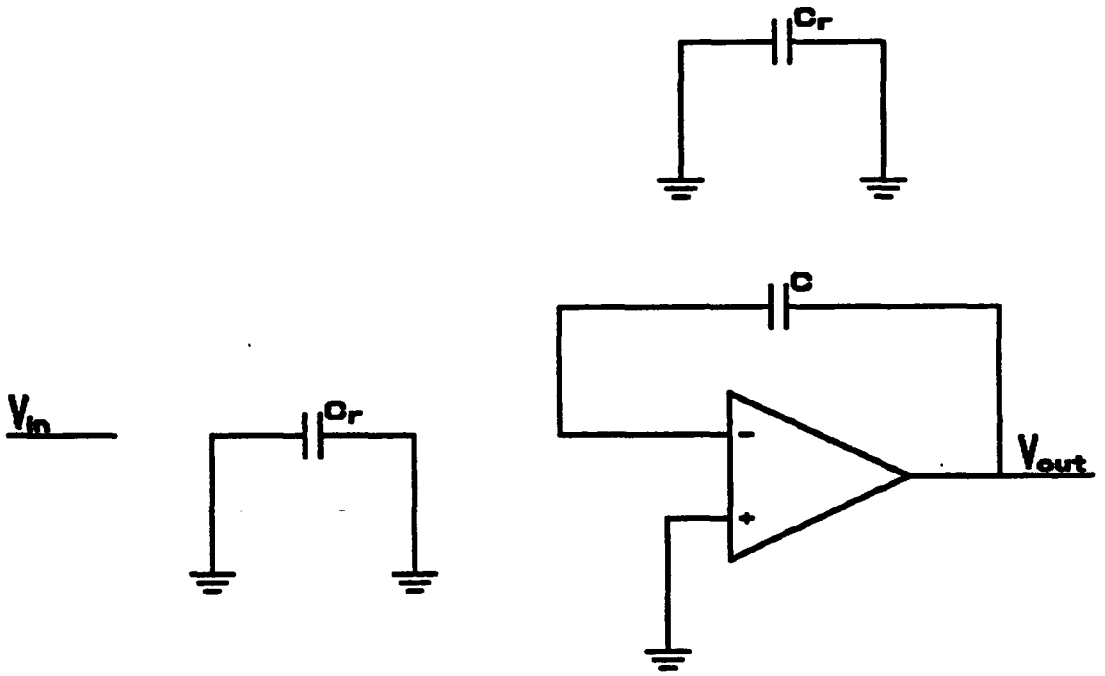

Figure 4.8 Integrator Circuit With ϕ_1 Gates Closed

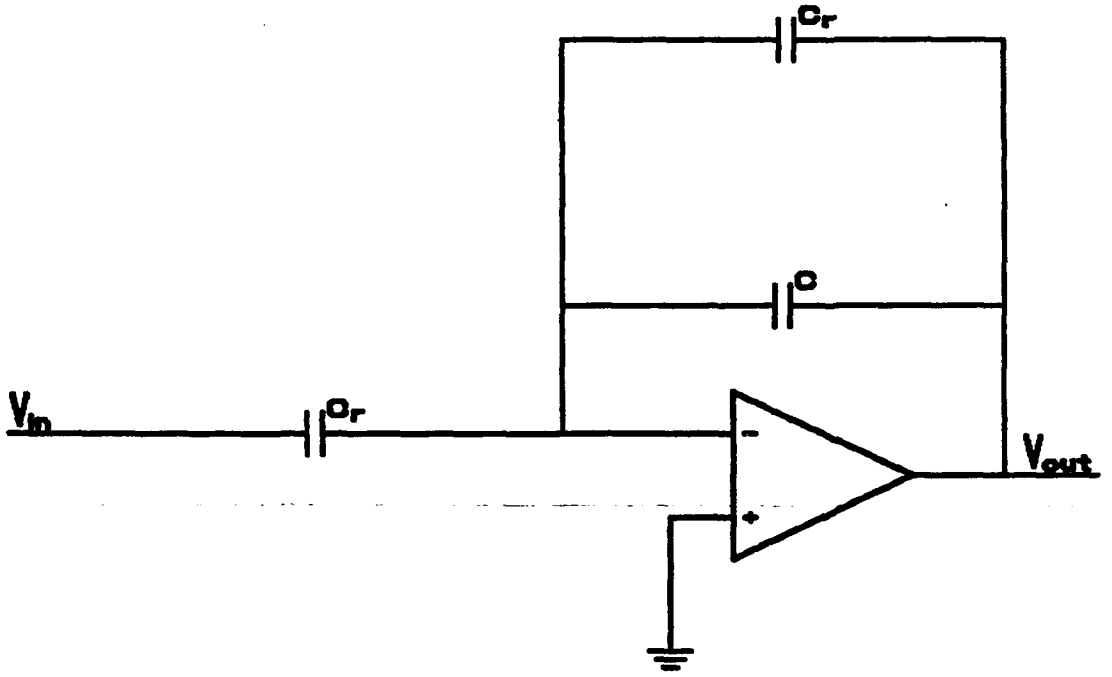

Figure 4.9 Integrator Circuit With ϕ_2 Gates Closed

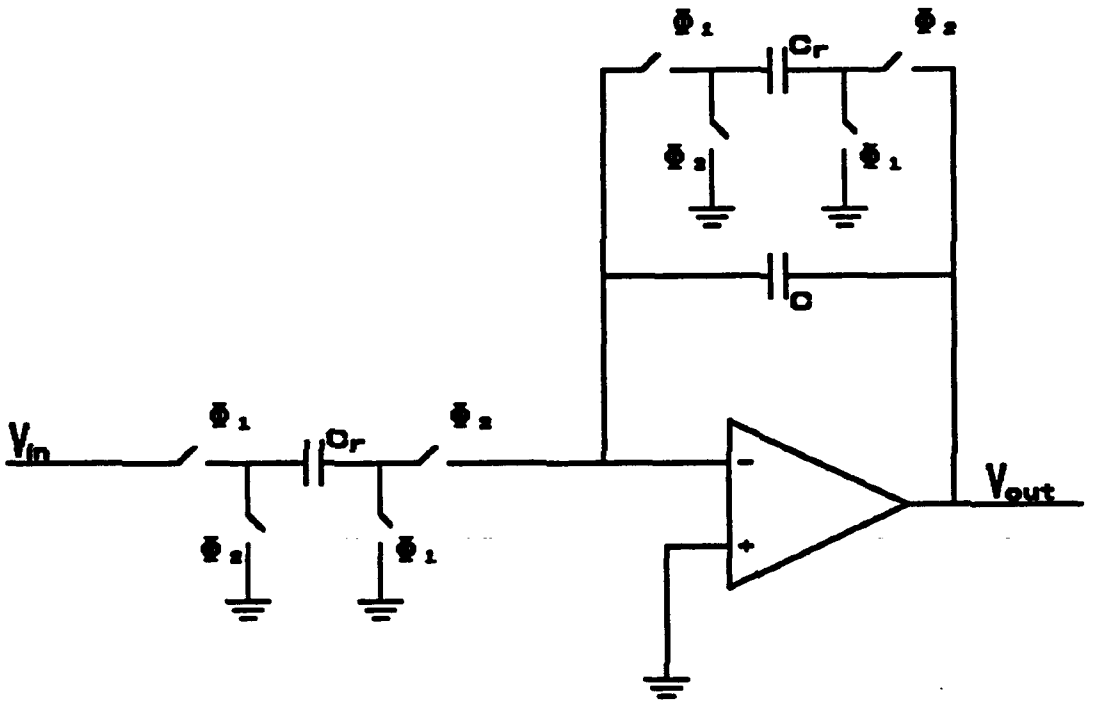

Figure 4.10 OFR Switched Capacitor designed Integrator Circuit

D. Z-DOMAIN ANALYSIS OF THE MODIFIED OPEN FLOATING RESISTOR

The z-domain analysis of the transfer function of the modified open floating resistor is obtained by obtaining the charge equations or the z-transform nodal equations on the network during the clock phases. Eight nodal equations exist for a four port switched capacitor block when analyzed in the z-domain. The general equation assumes a voltage potential on each port. The z-domain nodal charge relations for the first of the four nodes for an even clock phase is given by the following equation:

$$\Delta Q_1^e(z) = CV_1^e(z) - CV_2^e(z) - Cz^{-1/2}V_3^e(z) + Cz^{-1/2}V_4^e(z) \qquad (4.5)$$

The nodal charge relation for the odd clock phase is

$$\Delta Q_1^o(z) = 0 \qquad (4.6)$$

The nodal charge relation for the second node are similar with

$$\Delta Q_2^e(z) = -CV_1^e(z) + CV_2^e(z) + Cz^{-1/2}V_3^e(z) - Cz^{-1/2}V_4^e(z) \qquad (4.7)$$

for the even clock phase and

$$\Delta Q_2^o(z) = 0 \qquad (4.8)$$

for the even phase. The nodal charge relations for the third node are

$$0\Delta Q_3^e(z) = 0 \tag{4.9}$$

for the even phase and

$$\Delta Q_3^e(z) = -Cz^{-1/2}V_1^e(z) + Cz^{-1/2}V_2^e(z) + CV_3^e(z) - CV_4^e(z) \tag{4.10}$$

for the odd phase. The nodal charge relations for the fourth node are

$$\Delta Q_4^e(z) = 0 \tag{4.11}$$

for the even clock phase and

$$\Delta Q_4^e(z) = Cz^{-1/2}V_1^e(z) - Cz^{-1/2}V_2^e(z) - CV_3^e(z) + CV_4^e(z) \tag{4.12}$$

for the odd clock phase. In this modified OFR network the terminals at nodes one and two are connected to ground. This simplifies the preceding equations so that the first and second nodal equations are always equal to zero. The third and fourth nodal equations are modified such that the time delayed influences on the charges are removed. The modified third and fourth nodal relations are

$$\Delta Q_3^e(z) = 0 \tag{4.13}$$

$$\Delta Q_3^\circ(z) = CV_3^\circ(z) - CV_4^\circ(z) \qquad (4.14)$$

and

$$\Delta Q_4^\circ(z) = 0 \qquad (4.15)$$

and

$$\Delta Q_4^\circ(z) = -CV_3^\circ(z) + CV_4^\circ(z) \qquad (4.16)$$

The z-domain nodal relations have been reduced to the equivalent of a continuous resistor in the modified OFR network. The grounding of the first and second nodes has removed the delayed effects of the incomplete charges that would have otherwise been left on the nodes. These modified OFR switched capacitor networks will now be implemented into the composite op amp configuration.

E. SUMMARY

Switched capacitor networks can perform predictably and reliably when their parasitic capacitances are constrained to be ineffective. The parasitic capacitances of a switched capacitor network can be effectively eliminated by utilizing an appropriate circuit topology, such as the topology of the modified OFR network.

This parasitic free switched capacitor networks will now be implemented into a composite operational amplifier.

V. STRAY INSENSITIVE SWITCHED CAPACITOR COMPOSITE AMPLIFIERS

A. INTRODUCTION

The stray insensitive switched capacitor composite op amp network is a very interesting and a very useful composite of switched capacitor networks and active components. The switched capacitor realization of resistors allows more efficient use of IC area and more accurate component manufacturing, while the composite op amp increases the GBWP of the system and reduces the overall network active and passive sensitivities. Most active switched capacitor networks are frequency range limited due to the settling time of the op amps used in the circuit. MOS op amps can be designed with .5 micro second settling time to reach .1% of its final value to a step response. Based on this settling time, a 1 MHz clock was chosen to keep the switching frequency much greater than the signal frequency. This will allow for the relaxation of the requirements on the reconstruction filter and avoid warping of frequencies.

The general design approach of this thesis is an extension of the designs explained in [Ref. 2] and [Ref. 5]. The goal of this thesis is to implement the composite op amp with switched capacitor equivalent resistors as a finite gain amplifier and verify its performance against the continuous composite op amp performance. Then, this switched capacitor composite op amp will be implemented in a band pass filter and the results compared against the continuous band pass filter.

In this research, only the composite op amp is implemented with switched capacitors; the remainder of the network is implemented with continuous resistors and capacitors.

B. THE PROPOSED SWITCHED CAPACITOR COMPOSITE OP AMP

The basic components of the parasitic free switched capacitor C2OAs are the superior performing C2OAs and the modified OFR switched capacitor realization of a resistor whose parasitic free operation was established in the previous chapter. From the four C2OAs that showed superior continuous results, C2OA-1 was initially chosen and developed in a finite gain switched capacitor circuit. Subsequently C2OA-2 was also implemented in a finite gain switched capacitor circuit. The composite op amp implementation was accomplished with the substitution of the modified OFR switched capacitor network for each resistor in the composite op amp configuration, as shown in the implemented design of Figure 5.1. The switched capacitor composite op amp is constructed of two switched capacitors with their corresponding switches, one unswitched capacitor, and two LM741 op amps. The value of the switched capacitors were chosen to ensure the proportionality requisite to producing a maximally flat gain response. The value of Q for a maximally flat gain response is .7071. The value of α for the C2OA-1 can be determined with the value of Q and the equations in Table 2.2 to be 6.1. The measured switched capacitor values in the circuit were 130 pf and 730 pf. The unswitched capacitor was placed across the feedback loop of each op amp to ensure an open loop condition

did not occur. This capacitor value was measured at 46 pf. Verification of the GBWP was to be accomplished by choosing a gain of 100 and thus avoiding the limitations of the natural poles of the op amps. The continuous resistor values were chosen at 1 KΩ for the input resistor R_i, and 100 KΩ for the feedback resistor R_f. The finite gain switched capacitor circuit for the C2OA-1 is shown in Figure 5.2.

The implemented switched capacitor C2OA-2 circuit is shown in Figure 5.3. The maximally flat gain response criteria determined the value of α to be 6.1. The measured switched capacitor values in the circuit were 46 pf and 252 pf. A gain of 100 was chosen to verify the GBWP against the previous results and also avoid the limitations of the natural poles of the op amps. The continuous resistor values were chosen at 1 KΩ for the input resistor R_i, and 100 KΩ for the feedback resistor R_f. An unswitched capacitor was placed across the feedback loop of each op amp to ensure an open loop condition did not occur. These capacitor values were approximately 70 pf. Changing the absolute values of the switched capacitors did not measurably affect the circuit as long as the value of α remained constant. This demonstrated the dependence of the composite op amp on the relative value of α. The experimental results will be shown in the next chapter.

Finally the switched capacitor C2OA-1 was implemented in a band pass filter circuit. The flat gain response was implemented with the value of α equal to 6.1. The components exterior to the composite op amp were continuous elements. R_1 was chosen at 100 Ω, R_2 was chosen at 16 KΩ and R_3 was chosen at 5.6 KΩ. C_1 was chosen at 8 nf and C_2 was chosen at 260 pf. The output signal goes through a low

pass filter comprised of R_3 and C_2 to remove much of the clock signal from the output signal.

The implemented circuit is shown in Figure 5.4. The value of the ratio, α, remained the same for the band pass filter circuit; however, the values of the switched capacitors were changed. For the band pass filter circuit the switched capacitor values were 259 pf and 1.61 nf.

The circuit diagram for the switched capacitor C2OA-1 is contained in Figure 5.5, and the circuit diagram for switched capacitor C2OA-2 is contained in Figure 5.6.

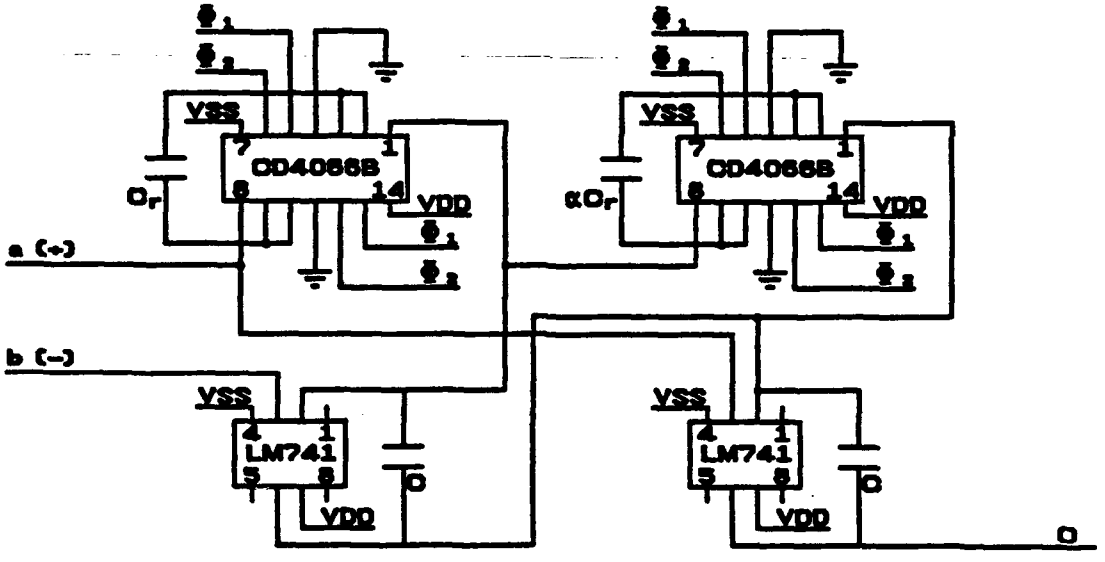

Figure 5.1 Switched Capacitor C2OA-1 Configuration

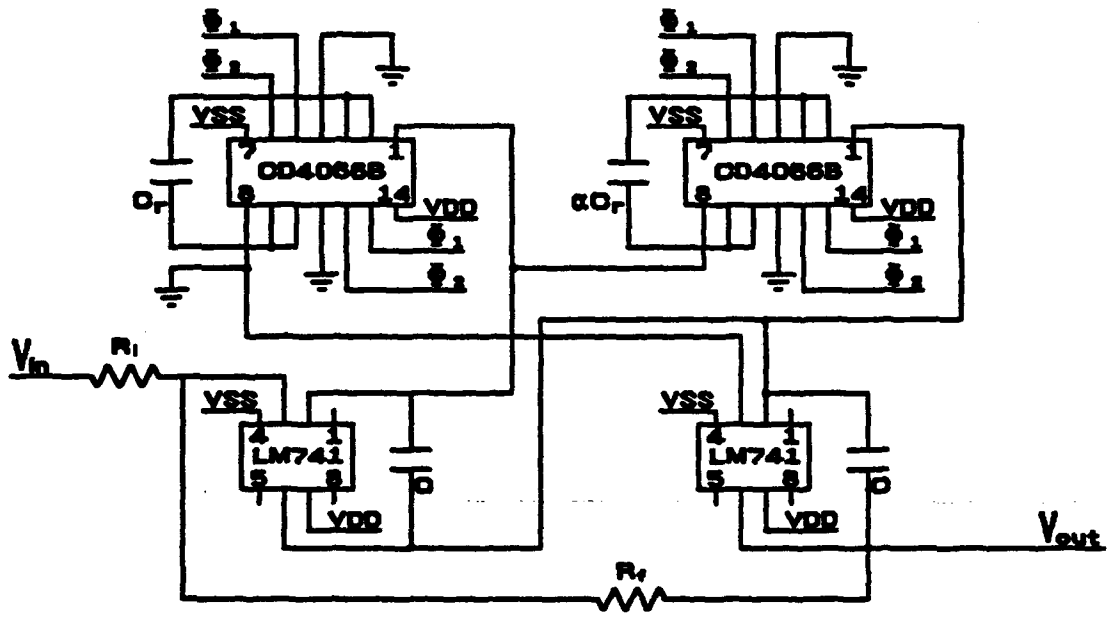

Figure 5.2 Finite Gain Switched Capacitor C2OA-1 Configuration

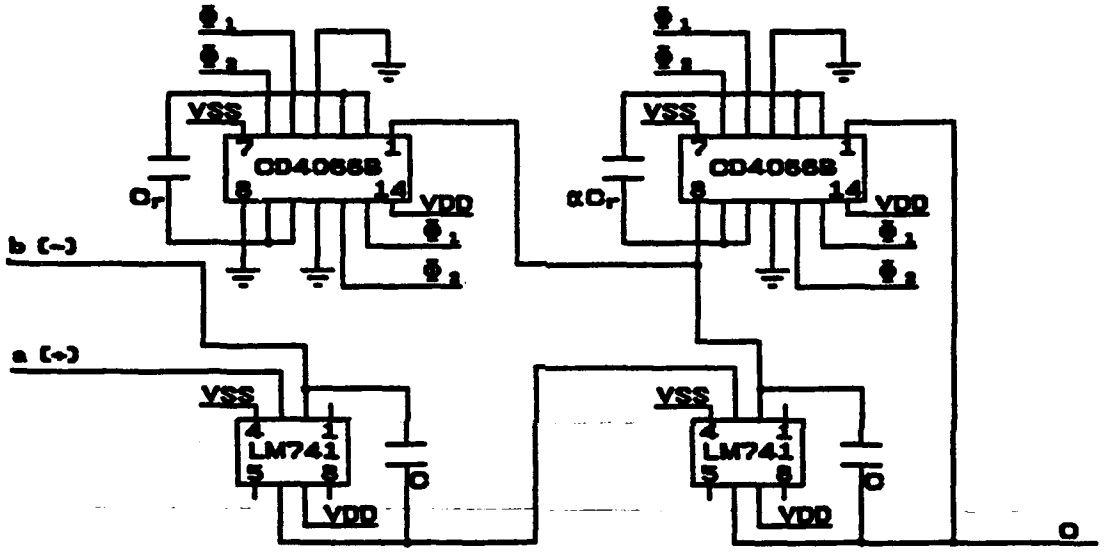

Figure 5.3 Switched Capacitor C2OA-2 Configuration

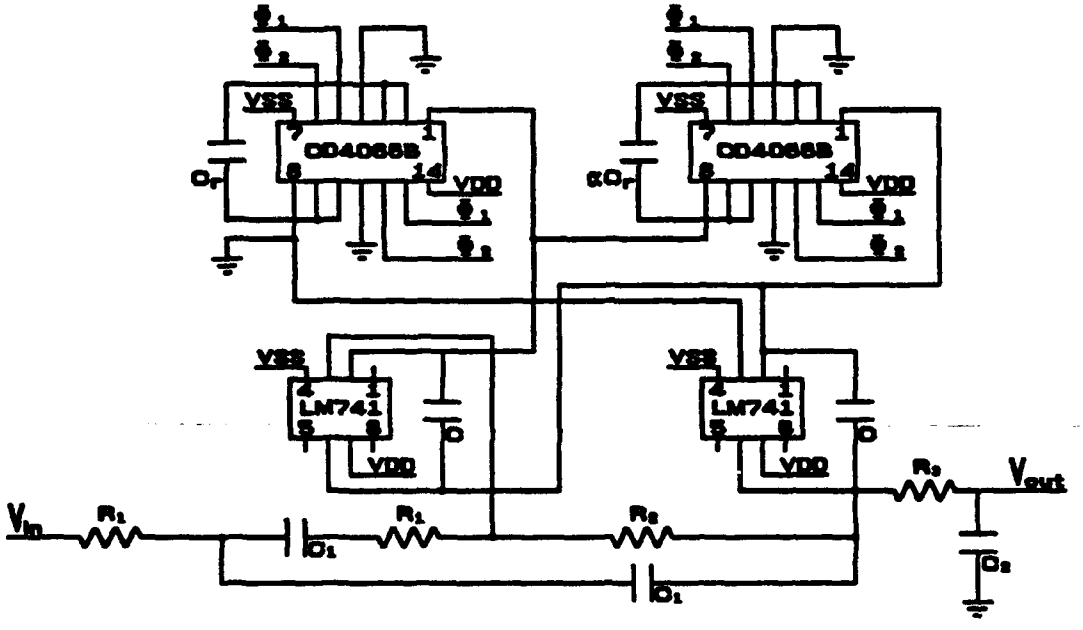

Figure 5.4 Bandpass Switched Capacitor C2OA-1 Configuration

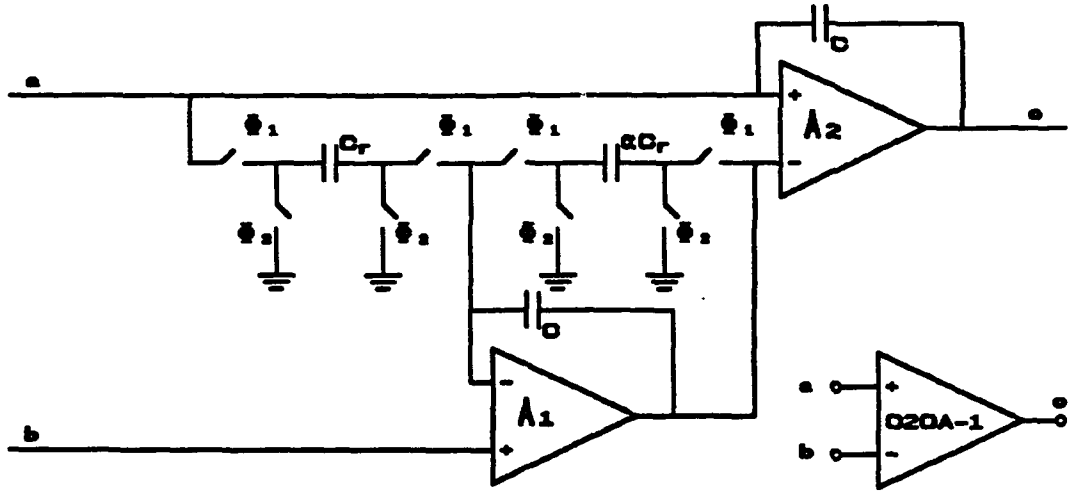

Figure 5.5 Modified OFR C2OA-1 Circuit

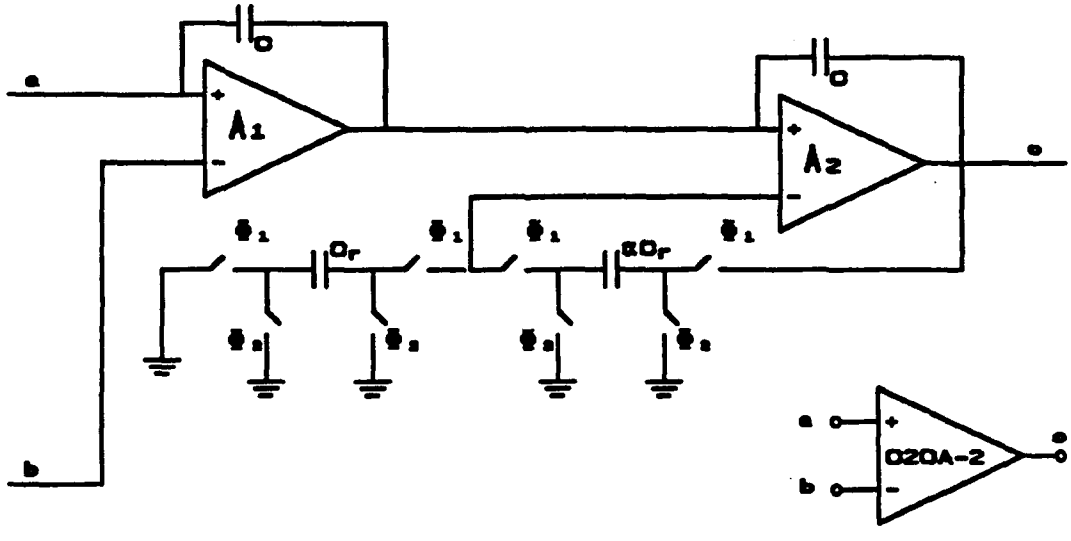

Figure 5.6 Modified OFR C2OA-2 Circuit

VI. EXPERIMENTAL RESULTS

A. THE STRAY INSENSITIVE SWITCHED CAPACITOR COMPOSITE OPERATIONAL AMPLIFIER IMPLEMENTATION

The parasitic free switched capacitor composite op amp in the finite gain circuit was implemented as designed in Chapter V. The 1 MHz, two phase nonoverlapping clock input signal was generated by a Hewlett Packard 3312A Function Generator, using the design discussed in Chapter III. The magnitude of the clock signal was set to plus or minus five volts. The power supply for the networks was provided by a Tektronix PS 503 A Dual Power Supply. The magnitude of V^+ was set at plus seven volts and the magnitude of V^- was set at minus seven volts. The input signal was a sine wave generated by an Exact Model 120 Waveform Generator. A second input signal source used for the band pass filter implementation was a swept sine wave generated by a Tektronix 5L4N Spectrum Analyzer. This signal was used to test the frequency response of the networks. Measurements were taken on the Tektronix 5L4N Spectrum Analyzer, a Hewlett Packard 3561 A Dynamic Signal Analyzer and a Cos 6100 M Oscilloscope.

Some problems are present which may cause changes in the response of the network. These include

1. Capacitor values on the order of pico farads within the prototype board.

2. The measuring probes have some capacitive input impedance.

3. Grounding problems.

4. Equipment scaling problems.

5. Capacitor values change within their tolerance limits.

Measurements were taken and the results were compared with the results obtained by the continuous network of identical design. Clock feed through was seen as noise on the output signal. This noise can be reduced by feeding the output signal through a low pass filter as shown in Figure 5.4. This is designed to allow the signal to pass and block the higher clock frequency. Clock noise was also present in the circuit through the power cords of the equipment. This noise was significantly reduced by inserting one microfarad capacitors between V^+ and ground and between V^- and ground.

B. THE FINITE GAIN SWITCHED CAPACITOR COMPOSITE OPERATIONAL AMPLIFIER

The finite gain switched capacitor C2OA-1 circuit was implemented with a gain of 100. An input peak to peak signal voltage of 30 mv was produced by putting the Exact Model 120 signal through a finite gain op amp with a gain reduction of 100. The gain on the output of the circuit was 3 volts peak to peak as predicted. The continuous finite gain C2OA-1 circuit demonstrated a 3 dB frequency of 81.75 K Hz. The switched capacitor finite gain C2OA-1 circuit demonstrated a 3 dB frequency of 68.75 K Hz. In contrast, the 3 dB frequency of a single op amp in the same finite

gain configuration yielded a value of only 8 KHz. Figure 6.1 shows the continuous finite gain composite op amp signal over the switched capacitor composite op amp signal. The noise from the clock signal is visible in both the continuous and the switched capacitor signal. The noise on the continuous signal is due to the noise generated by the clock through the circuit board, rather than the clock feed through noise. The clock feed through noise is also apparent on the lower switched capacitor signal. The voltage scale for Figure 6.1 is one volt per division, where the signals measure four volts peak to peak. The addition of a low pass filter removes much of the clock associated noise as seen in Figure 6.2. The upper signal is the original switched capacitor composite op amp output signal and the lower signal is the same signal after being fed through a low pass filter.

The implementation of the C2OA-2 into the finite gain circuit showed similar results. The 3 dB frequency was 69.5 KHz. Both the C2OA-1 and the C2OA-2 circuits showed a decrease of about 10 KHz from the anticipated results in the 3 dB frequency. This deviation is probably due to the problems previously mentioned.

C. BANDPASS SWITCHED CAPACITOR COMPOSITE OPERATIONAL AMPLIFIER FILTER

The band pass switched capacitor C2OA-1 filter was implemented as designed in Chapter V. A swept sine wave input generated by the Tektronix *5LAN Spectrum* Analyzer was applied to both the continuous and the switched capacitor band pass filter. The continuous filter demonstrated a center frequency of 15.55 KHz. The

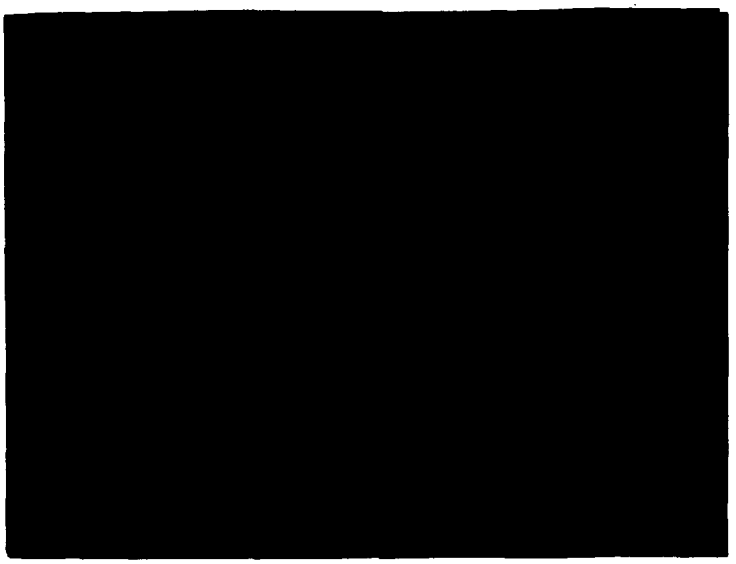

Figure 6.1 Continuous (Upper) and Switched Capacitor (Lower) Finite Gain Response

upper and lower 3 dB frequencies of this circuit were 17.15 KHz and 13.85 KHz respectively which corresponds to a filter quality factor of

$$Q = \frac{15.55}{17.15 - 13.85} = 4.7 \qquad (6.1)$$

The frequency response of the continuous filter is shown in Figure 6.3.

The measured center frequency of the switched capacitor filter was 15.85 KHz. The upper and lower 3 dB frequencies of this circuit were 17.75 KHz and 14.45 KHz respectively which corresponds to a filter quality factor of

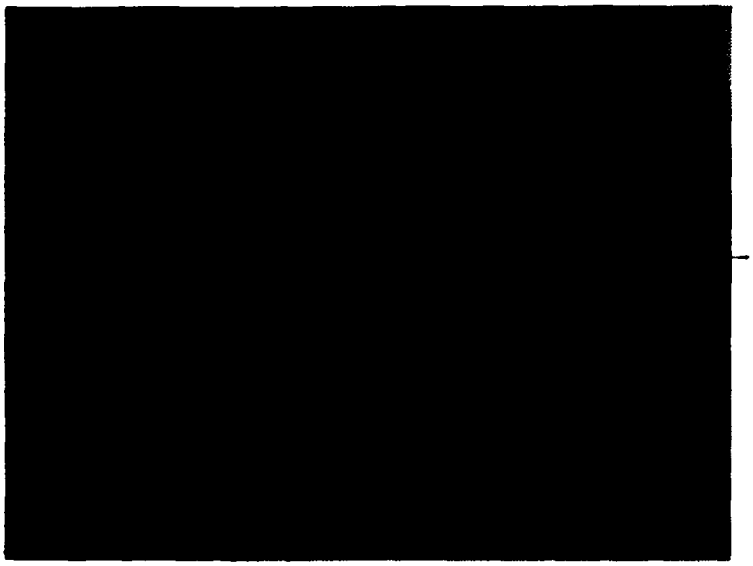

Figure 6.2 Unfiltered (Upper) and Filtered (Lower) Switched Capacitor Output Signals

$$Q = \frac{15.85}{17.75 - 14.45} = 4.8 \qquad (6.2)$$

The frequency response of the switched capacitor filter is shown in Figure 6.4. The center frequency differed by approximately 300 Hz. A superimposed plot of both frequency responses is shown in Figure 6.5. The plot of the switched capacitor frequency response has been translated to allow the superposition of the plots. The slight variation in Q is again probably due to the problems stated earlier in the chapter.

Figure 6.3 Continuous Bandpass Filter Frequency Response

Simulated parasitic capacitances on the order of up to 50 percent of the capacitor value were introduced in to the circuit and produced no measurable change in the response of the circuit. This verifies the stray insensitive characteristics of the network.

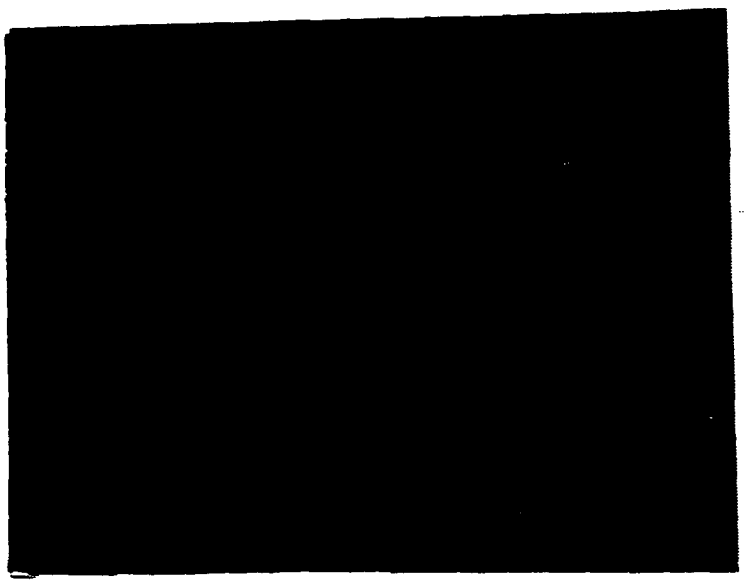

Figure 6.4 Switched Capacitor Bandpass Filter Frequency Response

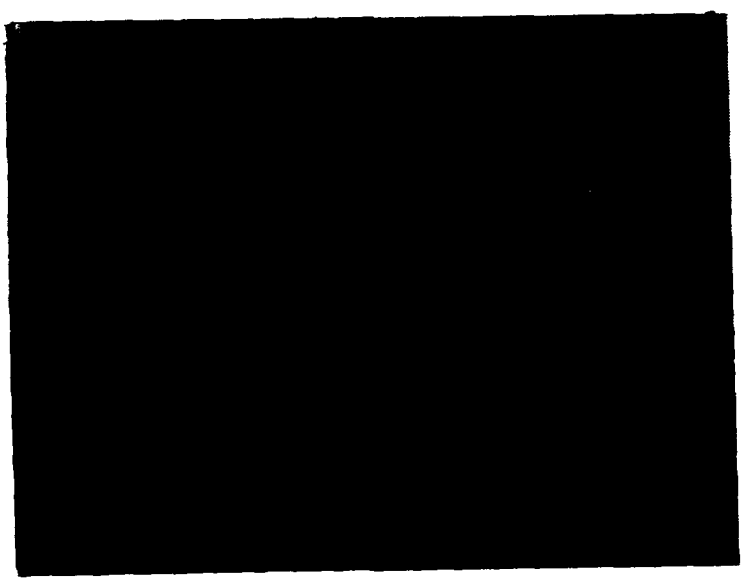

Figure 6.5 Superimposed Continuous and Switched Capacitor Filter Outputs

VII. CONCLUSIONS

The designs described in this thesis present a practical implementation of a parasitic free switched capacitor composite op amp that can be utilized in a variety of analog network applications. The parasitic free operation is accomplished through the appropriate placement of switches in the switched capacitor equivalent resistors. The modified OFR switched capacitor realization was instrumental in achieving these new designs. The composite op amp in a switched capacitor mode produces superior results that are nearly the equal of the continuous results. The design requires an accurate uniform clock signal for switches control. Experimental results showed the close agreement between the continuous and the switched capacitor results.

This research can be extended to develop a parasitic free switched capacitor wide band programmable filter using digitally programmable switches as presented in [Ref. 1]. The above newly developed switched capacitor composite op amp would be instrumental in such a realization. This study can also be applied to the VLSI implementation of this structure into a single chip. These novel designs would have great impact on the implementation of Neural Networks in integrated form [Ref. 8].

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